Abstracts

Circuit reduction technique for finding the steady state solution of nonlinear circuits

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Computing the steady state response of large nonlinear circuits is becoming a key simulation requirement due to the rapid market growth of RF silicon ICs. In this paper we describe a nonlinear circuit reduction algorithm for finding the steady state response. The proposed algorithm uses a congruent transformation-based technique to reduce the harmonic balance equations into a much smaller set of equations. The main feature of the reduced circuit is that it shares with the original one a certain number of the derivatives w.r.t. the RF input power. Steady state analysis is then done on the reduced circuit instead of the original circuit.

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